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SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR

Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code :T&T16EC5507

Branch& Specialization: ECE & VLSI**Year &Sem:** I M.Tech& II-Sem

UNIT –I

1. a) Explain the modeling digital circuit at register level and logical level.
   b) Explainhazard detection.
2. a)Explain in detail, external representation and internal representation instructural models of vlsi circuits.
   b) Explain about controlling value and inversion value for a combinational circuit. Discuss how the gate evaluation is carried out by input scanning.

3. a) List and explain level of modeling.
   b) With an example explain how hazards detected.

4. a) What are the different functional modeling techniques at the logic level? Explain about any two techniques.
   b) Write short notes on hazard detection.

5.a) Explain about structural modeling with example.
   b) Discuss about various types of simulation and delay models.

6.a) Explain about register level modeling with example.
   b) What is meant by hazards? Mention its types and how they are detected.

7. Discuss the register level and structural models.

8.a) Explain the logic simulation of applications?
   b) Write short notes on compiled simulation?

9.Explain about the delay model

10. Explain about element evaluation.

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UNIT –II

1. a)Explain about fault-detection and redundancy.
   b) Define the following fault models using examples.
   (i)cross-point fault (ii)multiple-stuck-at fault.

2.a) Explain what is meant by fault collapsingand discuss the importance of fault Collapsing.

b) Explain the methods of equivalence fault collapsing and dominant fault collapsing with suitable example.

3. a) Describe the source of fault mechanism.How the fault can be detected and located.

b)List and explain any two general techniques for combinational circuits.

4. a) Write a short note on fault modes.

b) Explain about redundant circuits.

5. a) Explain about logic fault models in detail.

b) Differentiate single stuck and multiple stuck at fault models.

6.a) Explain about fault redundancy in detail.

b) Given some of the applications of fault simulation.

7. a) List the general techniques for combinational circuits.

b)Explain about multiple stuck-fault modes.

8. a) Explain fault equivalence and fault location.

b) Explain about multiple stuck-fault models.

9. a) Explain about on single stuck fault models.

10.a) Write a short notes of simulation application.

b) Basic issues of testing for single stuck faults.

UNIT –III

DESIGN FOR TESTABILITY

1. (a)Explain the Generic Boundary Scan [5M]
   (b)Discuss the system level DFT approaches [5M]
2. (a)List out the Scan testing methods [5M]
   (b) Write Short notes on absorbability [5M]
3. Explain about testability trade-off [10M]
4. (a)Differentiate between board level and system level DFT approaches [5M]
   (b)Explain about syndrome test in detail [5M]
5. (b)Explain about system level DFT approaches [10M]
6. (a)Write the features of compression technique [5M]
   (b)Expression signature analysis [5M]
7. (a)How to perform syndrome test and signature analysis in digital circuits [5M]
   (a) How is generic boundary scan handled [5M]
8. Explain about storage cells for scan design [10M]
9. Differentiate between generic boundary scan and full integrated scan [10M]
10. (a)Explain about board level and system level DFT approaches [5M]
    (b)Explain about syndrome test and signature analysis [5M]

UNIT-IV

BUILT-IN SELF -TEST

1. Explain the trade-off between ATES and BIST [10M]
2. a) Discuss the different errors/faults that are associated with memory operation [5M]
   b) Explain advanced BIST concepts [5M]
3. a) Explain any two BIST concepts [5M]
   b) What is CATS? Explain? [5M]
4. a) Write short notes on BEST and RTS [5M]
   b) Discuss the steps involved in design for self-test at board level [5M]
5. a) Explain the architecture of LOCST and RTD [5M]
   b) List JTAG testing features. [5M]
6. a) Explain about BIST and name the architecture present in it [5M]
   b) Give the design for self-test at board level [5M]
7. Explain any two BIST architectures
   a) CSBL [4M]
   b) LOCST [3M]
   c) RTD [3M]
8. a) Explain BIST architectures of LOCST,RTD [5M]
   b) CSTP-BIST architecture [5M]
9. a)Explain design for self-test at board level [5M]
   b) Write short notes on STUMPS [5M]
10. a)Write a short notes on CSBL and BEST architecture [5M]
    b) Explain about the self-test at board level [5M]

UNIT-V
MEMORY BIST (MBIST)

1. Write a brief notes on
   a) JTAG testing features [5M]
   b) Signature analyser [5M]
2. Describe in detail about any one architecture for memory BIST [10M]
3. a)Explain the basic concepts of in circuit testing (ICT)and what are the advantages and disadvantages [5M]
   b)What are the requirements for carrying out in circuit testing of a circuit board [5M]
4. a)List and explain memory test requirements for MBIST [5M]
   b)Explain any two types of memories and Integration [5M]
5. a)What is meant by embedded core testing ?Explain [5M]
   b)Explain ICT [5M]
6. a)With an example of explain embedded core testing [5M]
   b)Write short notes on types of memories [5M]
7. a)Explain signature analysis [5M]
   b)List JTAG testing features [5M]
8. Explain about the memory test requirements for MBIST [5M]
9. a)Give a short notes on automatic in circuit testing. [5M]
   b)Write down the important features of JTAG testing. [5M]
10. Explain embedded memory testing model. [10M]

Prepared by: **VijayaBhaskar C**